UNIVERSAL GATES FOR ICs AND TRANSFORMATION

OF NETLISTS FOR THEIR IMPLEMENTATION

ABSTRACT OF THE DISCLOSURE

An original netlist is transformed to one
5   employing universal gates. A negation net is created
for each net coupled to an input or output of each
gate and an input of each inverter in the original
net. Each gate is removed from the original netlist
and a universal gate is inserted so that the nets
10 previously coupled to the inputs and output of the
removed gate and a negation of those nets are coupled
to the inputs and outputs of the inserted universal
gate in a selected arrangement. Each inverter is
removed from the original netlist and the net
15 previously coupled to the input of the inverter is
negated. A universal gate comprises gates performing
anding and oring functions whose inputs and outputs
are selectively coupled to the nets of the original
netlist, and their negations.

20